REMARKS

In the Office Action, Claims 1-2 and 4-15 were rejected under 35 U.S.C. §102. Claims 1, 2 and 4-15 are pending in the present application. Claims 1, 2, 4 and 5 have been amended herein. Claims 9 and 15 have been cancelled without prejudice or disclaimer. No new matter has been added by any of the amendments made herein. Applicants respectfully submit that the rejections have been overcome or are improper for at least the reasons set forth below. This Amendment is submitted with a Request for Continued Examination ("RCE"). A check in the amount of $790.00 is submitted herewith to cover the cost of the RCE. Please charge Deposit Account No. 02-1818 for any insufficiency or credit. Accordingly, Applicants respectfully request reconsideration of the patentability of Claims 1, 2, 4-8 and 10-14.

Claims 1, 2 and 4-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,734,568 to Watanabe et al. ("*Watanabe I*"). Applicants respectfully disagree with and traverse this rejection because *Watanabe* does not disclose, teach, or suggest each and every element of the claimed invention.

Of the pending claims at issue, Claims 1, 2, 4 and 5 are the sole independent claims. As amended, Claim 1 recites, at least in part, a memory section including a first area for storing data of at least one user and a second area set in an unused area of said first area, said second area used by said at least one user stored in said first area and managed in a block unit having a predetermined size, and storing plural data for respectively prescribing different access rights to said at least one user in said first area, wherein the block unit includes a plurality of blocks that include a first block number and a second block number, said first and second block numbers reflecting the size of the memory area associated with each user based on the actual amount of information stored for each user. Claims 2, 4 and 5 include similar amendments intended to clarify that the size of the memory area associated with each user is not a predetermined amount, and rather is based on the amount of information stored for a user. Therefore, utilization efficiency of the memory is enhanced.

Watanabe I is directed to an IC card or smart card which can set security levels for each memory area in the card. (See the Abstract). Specifically as shown in Fig. 4, the memory area includes a plurality of index areas 1 through Y and a plurality of memory areas 1 through Y which correspond to each of the index areas. The index areas are used to access the

corresponding memory areas. See, *Watanabe I*, col. 3, lines 20-30. Furthermore, each index area as shown in Fig. 5, includes an area consisting of eight bits for storing different information. Specifically, each index area stores a head address of the corresponding memory area, an area consisting of six bits for setting the security level used to access writing and reading operations of the data stored in the memory area, an area consisting of eight bits for recording a record length in the corresponding memory area, an area for recording the maximum number of records assigned to the memory area and an area for recording the number bytes of the flagged bits located in the head address. See, *Watanabe I*, col. 3, lines 31-48.

However, as mentioned above, *Watanabe I* is primarily focused on setting multiple security levels and does not disclose an information processing apparatus or method with a memory section as required by the claimed invention. Indeed, the present disclosure discusses problems with prior memory utilization methods, such as that disclosed in *Watanabe I.* See, Specification, pg. 2, lines 3-10. When memory is managed in a predetermined storing unit, such as the memory unit assigned in *Watanabe I*, and data having a smaller size is stored in this area, unused memory is caused and utilization efficiency of memory is reduced. See, *Watanabe I*, Fig. 5.

Accordingly, *Watanabe I* does not disclose, teach or suggest "a memory section including a first area for storing data of at least one user and a second area set in an unused area of said first area, said second area used by said at least one user stored in said first area and managed in a block unit having a predetermined size, and storing plural data for respectively prescribing different access rights to said at least one user in said first area, wherein the block unit includes a plurality of blocks that include a first block number and a second block number, said first and second block numbers reflecting the size of the memory area associated with each user based on the actual amount of information stored for each user" as defined by amended Claim 1. Claims 2, 4 and 5 each include similar elements to amended Claim 1.

Therefore, for at least the reasons provided above, *Watanabe I* does not disclose, teach or suggest the elements of Claims 1, 2, 4 and 5, and Claims 6-8 and 10-14, which depend from these claims, respectively. Accordingly, Claims 1, 2, 4-9 and 10-14 are each patentably distinguished over *Watanabe I* and are in condition for allowance.

Claims 1, 2 and 4-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,849,614 to Watanabe et al. ("*Watanabe II*"). Applicants respectfully disagree with and traverse this rejection because *Watanabe II* does not disclose, teach, or suggest each and every element of the claimed invention.

Watanabe II is related to *Watanabe I* described above and teaches a composite IC card for controlling information of a plurality of different enterprises using the card in which a memory is divided into plurality of storage areas. The IC card also includes a code store section for storing a plurality of codes necessary to access the storage areas. See, *Watanabe II*, Abstract. Similarly to *Watanabe I, Watanabe II* includes a memory area having a plurality of index areas 1 through X and a plurality of storage areas 1 through X which are associated with each index area. See, *Watanabe II*, Fig. 1. As shown in Fig. 3, each index area is divided into storage area definition information and storage area control information. See, *Watanabe II*, col. 6, lines 42-55. Each storage area includes a first record to Mth record. The information is stored for each record and the record length is predetermined or "before hand set" so as to be written as the storage area definition information of each index area. As averred to on page 4 of the Office Action, the sixth byte of the index area defines the storage length. See, *Watanabe II*, col. 7, line 56.

Accordingly, for the same reasons provided above with respect to *Watanabe I*, *Watanabe II* does not disclose, teach or suggest a first area managed by a block unit where the block unit includes a plurality of blocks that include a first block number and a second block number, said first and second block numbers reflecting the size of the memory area associated with each user based on the actual amount of information stored for each user. Therefore, Claims 1, 2 and 4-8 and 10-14 are each patentably distinguished from *Watanabe II* and are in condition for allowance.

In light of the above, Applicants respectfully submit that Claims 1, 2 and 4-8 and 10-14 are patentable over the art of record because neither of the *Watanabe* references disclose, teach or suggest the elements of these claims. Therefore, Applicants request withdrawal of the anticipation rejections.

Accordingly, Applicants respectfully request that Claims 1, 2 and 4-8 and 10-14 be deemed allowable at this time and that a timely notice of allowance be issued in this case.

Respectfully submitted,

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